Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7107/7109 Family

1. INTRODUCTION

Most of Intersil's one chip A/D converters offer differential input, differential reference and separable analog and digital ground references. The price of all this freedom, of course, is technical vigilance, and this note is intended as a defense manual against the potholes and landmines it makes accessible. The discussion is based on the ICL7106/7, but applies in large part to the ICL7116/7, the ICL7126, the ICL7109, and to a lesser extent to the ICL7135.

2. GENERAL DESCRIPTION

Figure 1 shows the Block Diagram of the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

1. Auto-Zero Phase

During Auto-Zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10 μV.

2. Signal Integrate Phase

During signal INTegrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between INHI and INLO for a fixed time. This differential voltage can be within a wide common mode range — within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, INLO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase the polarity of the integrated signal is determined.

3. De-Integrate Phase

The final phase is DE-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$1000 \left(\frac{V_{in}}{V_{ref.}} \right)$$

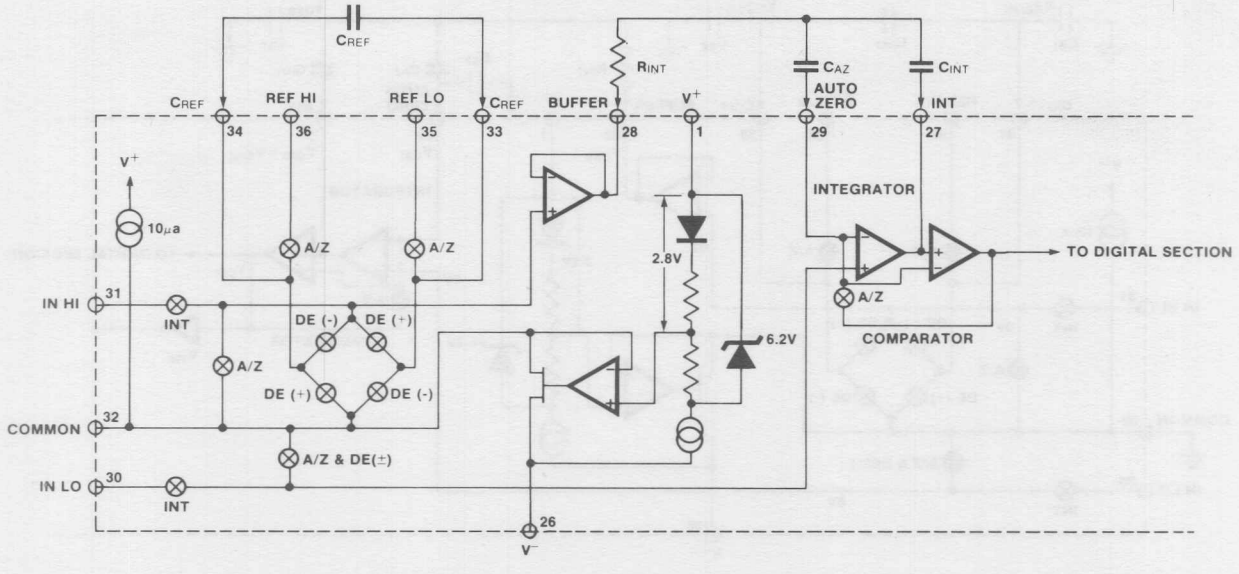

Figure 1. Analog Section of 7106/7107

3. CMRR AND COMMON MODE VOLTAGE EFFECTS

There are three basic voltages applied to the ICL7106/7, etc. which can give "common mode voltage" consequences. These are indicated in Figures 2, 3, and 4 which show the analog section in the phases described above. The choices are 1) of reference voltage source to COMMON, 2) of input voltage source to COMMON, and 3) of COMMON to (digital) supply voltage.

During Auto-Zero, the outputs of the buffer, integrator, and comparator are all within various offset voltages of analog COMMON. These are marked on Figure 2, which shows the Auto-Zero phase. For the remainder of the discussion, these offset voltages will be ignored, since they are merely added to other voltage changes described. The non-inverting inputs of the buffer and integrator are also tied to analog COMMON, so it is convenient to describe all these voltages with respect to COMMON.

1. Reference Common Mode Voltage to COMMON

The reference capacitor is recharged during the Auto-Zero time; the stray capacitance shown in Figure 2 as CS1 and CS2 will also be charged. During DE-integrate (Figure 4) the reference capacitor is switched so that one or the other of its terminals is at analog COMMON. This will cause charge-sharing with the stray capacitances on the other terminal. In particular, a common mode voltage on the reference input (with respect to COMMON) will give a roll-over error, since the effective DE-integrate reference will be higher in one polarity than the other. The ideal here is for $(V_{REFHI} + V_{REFLO}) = 2\ V_{ANCOM}$, at least for equal stray capacitances, but this is inconvenient in most applications. The roll-over error contribution at full scale (ignoring a second order term) is

$$2000\ \frac{(V_{REFLO}\ C_{S1} + V_{REFHI}\ C_{S2})}{V_{REF}\ C_{REF}} \simeq$$

$$2000\ \frac{V_{CM}\ (C_{S1} + C_{S2})}{V_{REF}\ C_{REF}}\ \text{(counts)}$$

For $C_{REF} = 0.1\ \mu F$, $C_S = 15pF$, $V_{CM}/V_{REF} = 10$, this can give two counts of error, but if $V_{REFLO} = 0$, and C_{S2} is 5 pF, the error is 0.1 counts, lost in the noise level. In the latter case (a very common application condition) C_{S1} does not contribute any errors, so putting the "outside foil" of the reference capacitor to this side will minimize roll-over. Also increasing C_{REF} (without corresponding increases in C_S) will reduce roll-over. Note that stray capacitance to the buffer output is also unimportant if either REFHI or REFLO is at COMMON.

2. Input Voltage to COMMON

First, the direct CMRR of the buffer and integrator op amps will themselves lead to a scale factor error and an offset if INLO is not at analog COMMON. Higher order CMRR terms are generally negligible, and this first order term is very small for most devices. It can be adjusted out in most applications with a reference voltage adjustment. More serious is the effect of stray capacitance to ground of the integrating and auto-zero capacitors, and the AZ pin, C_{S4} and C_{S3} in Figure 2. The AZ pin will swing from COMMON to INLO (Figure 3) and C_{S3} will have to be charged through C_{AZ}, giving an error voltage on C_{AZ}, during the integrate phase, of:

$$\Delta\ V_{AZ} = V_{INLO}\ \frac{C_{S3}}{C_{AZ}}$$

This acts as an offset voltage referred to the input, and is most serious for small ratios of full-scale input voltage to common mode voltage: For $C_{AZ} = 0.47\ \mu F$, $C_{S3} = 10pF$, $V_{INLO} = 2V$, the offset will be 40 μV, or 0.4 counts for 200 mV full scale input. This charge is recovered in the transition back to COMMON

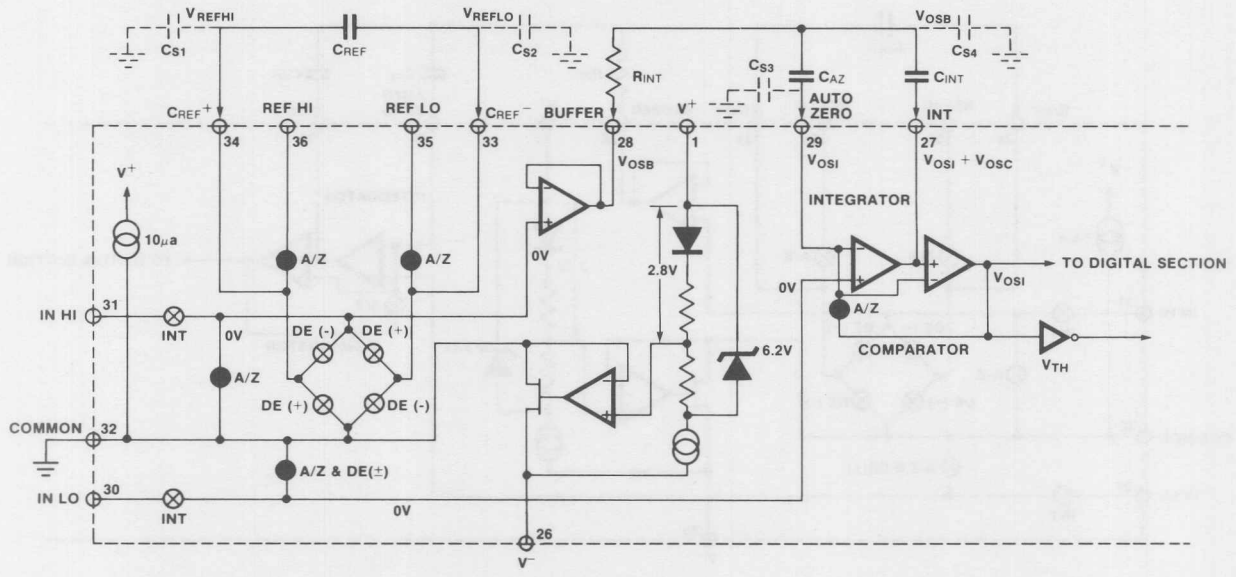

Figure 2. Auto-Zero Phase, with Offset Voltages and Stray Capacitances

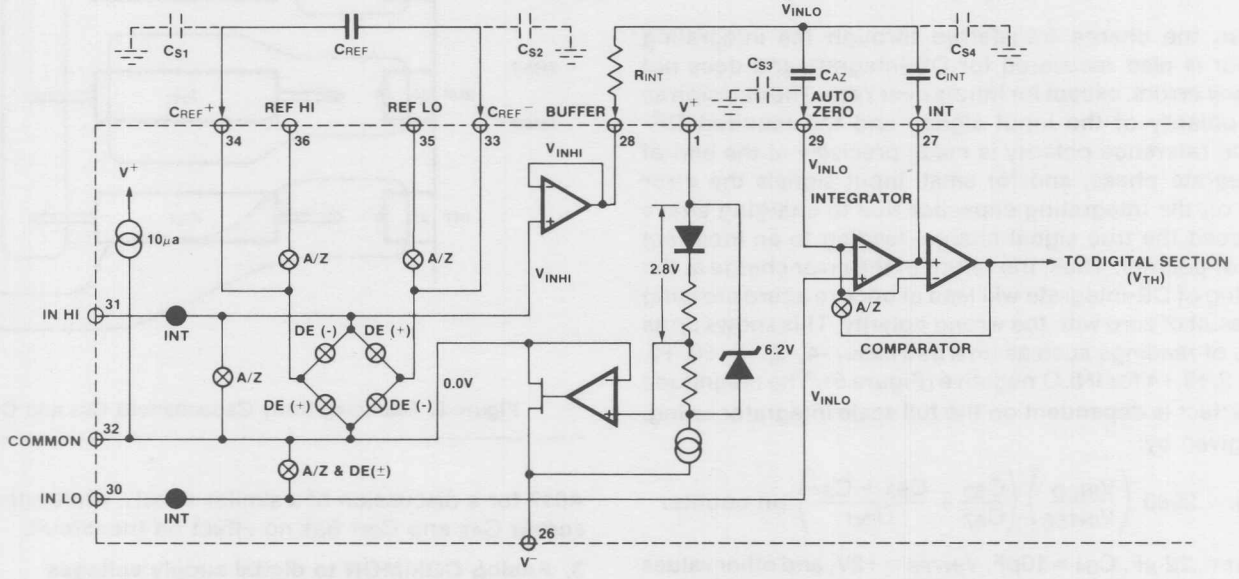

Figure 3. Integrate Phase. All voltages shown with respect to COMMON.

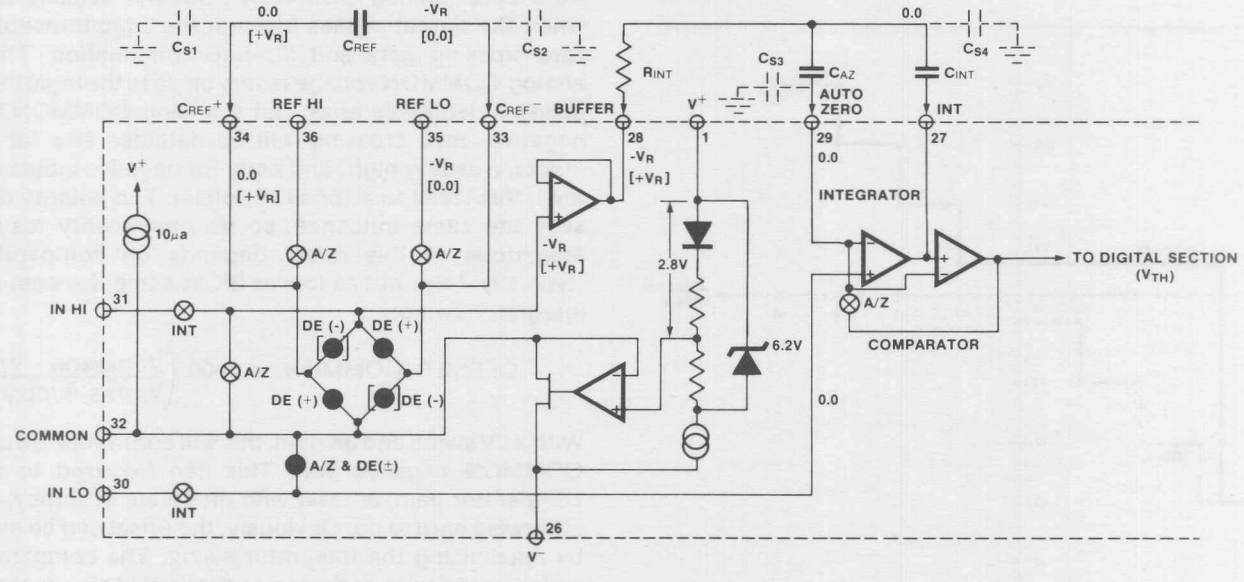

Figure 4. DE-integrate Phase. Voltages shown with respect to COMMON, for positive input. [ ] shows values for negative input.

for DE-integrate (Figure 4), so the offset is not continued in this phase. The same charge, together with that due to C_{S4}, also flows through the integrating capacitor. Ignoring second-order terms, the error voltage on the integrator output during the integrate phase will be:

$$\Delta V_{INT} = V_{INLO}\left(\frac{C_{S3}}{C_{AZ}} + \frac{C_{S3} + C_{S4}}{C_{INT}}\right)$$

However, the charge transferred through the integrating capacitor is also recovered for DE-integrate and does not cause any errors, except for inputs near zero. The decision as to the polarity of the input signal, and the required DE-integrate reference polarity is made precisely at the end of the integrate phase, and for small input signals the error charge on the integrating capacitor due to charging strays can exceed the true signal charge, leading to an incorrect choice of polarity. Thus, the return of the error charge at the beginning of DE-integrate will lead at once to a zero crossing and a result of zero with the wrong polarity. This shows up as a series of readings such as (in a bad case) -4, -3, +0, +0, +0, +0,+1,+2,+3,+4 for INLO negative (Figure 5). The magnitude of this effect is dependent on the full scale integrator swing, and is given by:

$$\Delta \text{ pol.} = 2000\left(\frac{V_{INLO}}{V_{INTFS}}\right)\left(\frac{C_{S3}}{C_{AZ}} + \frac{C_{S3} + C_{S4}}{C_{INT}}\right) \text{ (in counts)}$$

For C_{INT} = .22 μF, C_{S4} = 10pF, V_{INTFS} = +2V, and other values as before, this amounts to about 0.23 counts, but for C_{AZ} = 0.047 μF (recommended for 2.0V F.S.) Δ pol is 0.6 counts. A small increase in stray capacitance or reduction of integrator swing will give a significant "gap" in the readings, as shown in Figure 5. This effect, the only one causing significant non-linearity, can be reduced by guarding the integrating and auto-zero capacitors and resistor with either BUFFer out or INTegrator out pins in so far as possible. This can readily be done on a PC board by simple extension of the traces leading from those pins to the three components, as suggested in Figure 6. Note that excessive capacitance across R_{INT} will increase the width of the zero reading (see A017 for a discussion of a similar effect), while capacitance across C_{AZ} and C_{INT} has no effect on the circuit.

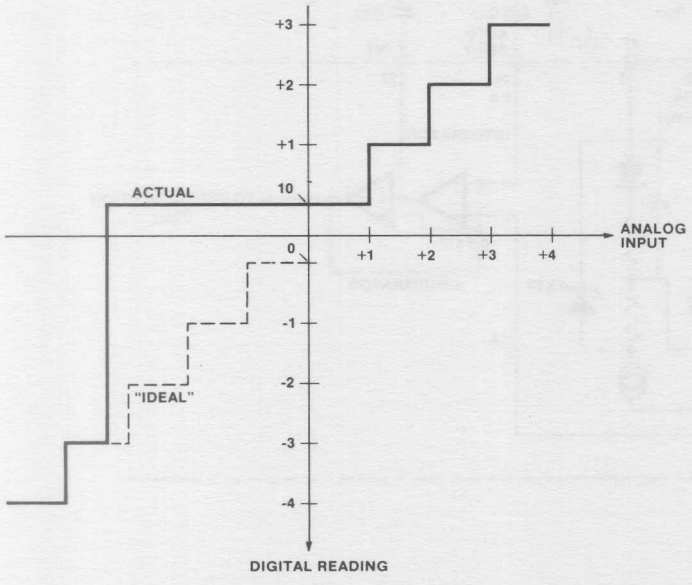

Figure 5. "GAP" in readings due to $V_{INLO} \neq$ COMMON (a bad case shown)

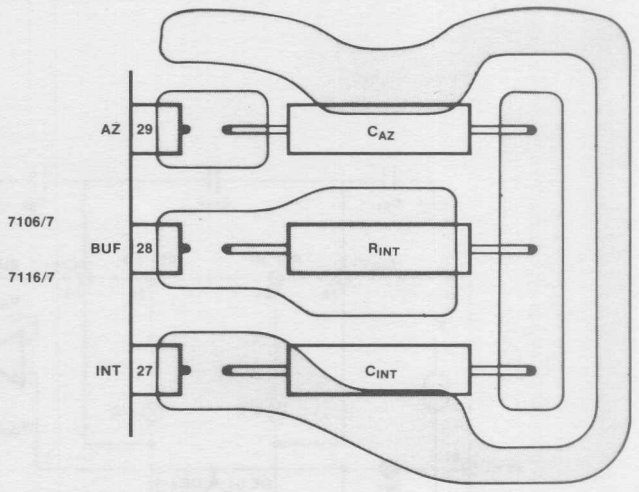

Figure 6. Reducing Stray Capacitances C_{S3} and C_{S4}

3. Analog COMMON to digital supply voltages

The COMMON line on the ICL7106/7 family of devices provides a convenient ground-return point in many applications; particularly with floating (battery) supplies. However, in a fixed supply environment, improved integrator swing (improving many system parameters) can be achieved if COMMON is pulled more negative, and the circuit has been set up to allow this. The effects described above are all independent of the actual level of COMMON, but the next one is not!

The DE-integrate phase should ideally terminate when the output of the comparator returns to the value it had during Auto-Zero (analog COMMON), but will actually terminate when the output passes through the logic threshold of the zero-crossing gate and flip-flop combination. The "free" analog COMMON voltage is very close to the logic threshold, giving a negligible error, but if analog COMMON is pulled negative, zero crossing will be detected late for positive inputs, (reading high) and early for negative inputs (reading low), this leads to a (positive) offset. The polarity detection sees the same influence, so no nonlinearity results. The magnitude of this offset depends on comparator gain (typically 7-8K, but as low as 3K in some devices) and F.S. integrator swing;

$$\text{OFFSET (COMMON)} = 2000\left(\frac{V_{COMMON} - V_{TH}}{V_{INTFS}\, A_{VCOMP}}\right)$$

With a 2V swing and 3K gain, this will contribute 1/3 count per COMMON negative volt. This can be used to measure comparator gain, at least with moderate accuracy, which is otherwise hard to do. Obviously, the offset can be minimized by maximizing the integrator swing. The comparator gain varies from device to device, and is limited also by the need to keep the comparator fast. Various improvements in this gain have been made, and will probably continue to be made in the future, but this offset should be considered carefully if COMMON is to be moved away from its "free" location, or if the logic supplies are altered.

4. The Auto-Zero Loop Residual

During the Auto-Zero phase, the converter self-corrects for all the offset voltages in the buffer, integrator, and comparator.

This section covers a normally undetectable, but under some circumstances significant, error generated in the auto-zero system. A similar effect which occurs in the 2-chip systems has been discussed previously (see A030, Appendix A), but the details and remedies are sufficiently different to warrant a separate discussion.

The relevant circuit to be discussed is shown in Figure 7 and the major cycle waveforms in Figure 8. Let us first assume that the prior auto-zero cycle has been indefinitely long, or is otherwise ideal, so that the conversion starts with no residual error on the auto-zero capacitor. The integrate and DE-integrate cycles will be classically perfect to the point at which a zero-crossing actually occurs (at the output of the integrator). However, from this point two delays occur; first the comparator output is delayed (due to comparator delay) and secondly the zero-crossing is not registered until the next appropriate clock edge. (For further discussion of this, see Application Note A017). At this point, the circuit is returned to the auto-zero connection (logic and switch delays may be absorbed in comparator delay as far as our discussion is concerned). The net result is that the integrator output voltage will have passed the zero-crossing point by an amount given by

$$V_{Ires} = \pm V_{IFS}\left(\frac{c_D + c_X}{C_{FS}}\right)$$

where $0 \leq c_X \leq 1$ is the variable delay, c_D is the fixed delay, C_{FS} is the full scale count in units of clock pulse periods, and V_{IFS} is the full scale integrator swing in volts.

Note: In all subsequent discussions, "C" indicates a capacitor, while "c" denotes a number (not necessarily an integer) of counts.

The range of this residual voltage corresponds to the integrator swing per count, and is independent of input value, except for polarity.

Note, however, that we have assumed a zero-crossing actually occurred. If the input is overloaded (past full scale), DE-integrate will terminate with a substantial residual voltage remaining on the integrator capacitor. The maximum value of this residual depends on the total possible swings of buffer and integrator, as compared to the "full scale" values used. In general, we may treat this case as corresponding to a large negative value of c_X.

The immediate effect of closing the auto-zero loop may be seen by examining Figure 7. We may consider the comparator as acting as an op-amp. Under these conditions: the voltage across the auto-zero impedance is high, and the (nonlinear) impedance is low; on the other hand, the initial voltage across the integrating resistor is zero.

Thus, the auto-zero capacitor will be charged rapidly to exactly cancel the residual voltage, as shown in Figure 9. The output of the integrator is now at the correct position, but the auto-zero and integrator capacitors have shared the original error. The junction point of the two capacitors and resistor has been moved by a portion of the original residual voltage, given by:

$$V_{AZI} = V_{Ires}\left(\frac{C_{INT}}{C_{AZ} + C_{INT}}\right) \qquad (4.1)$$

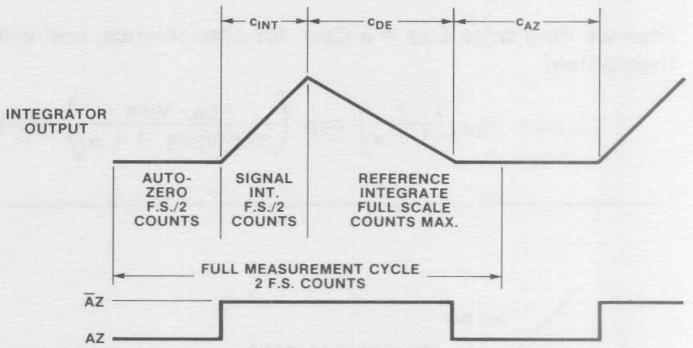

Figure 8. Major Cycle Waveforms

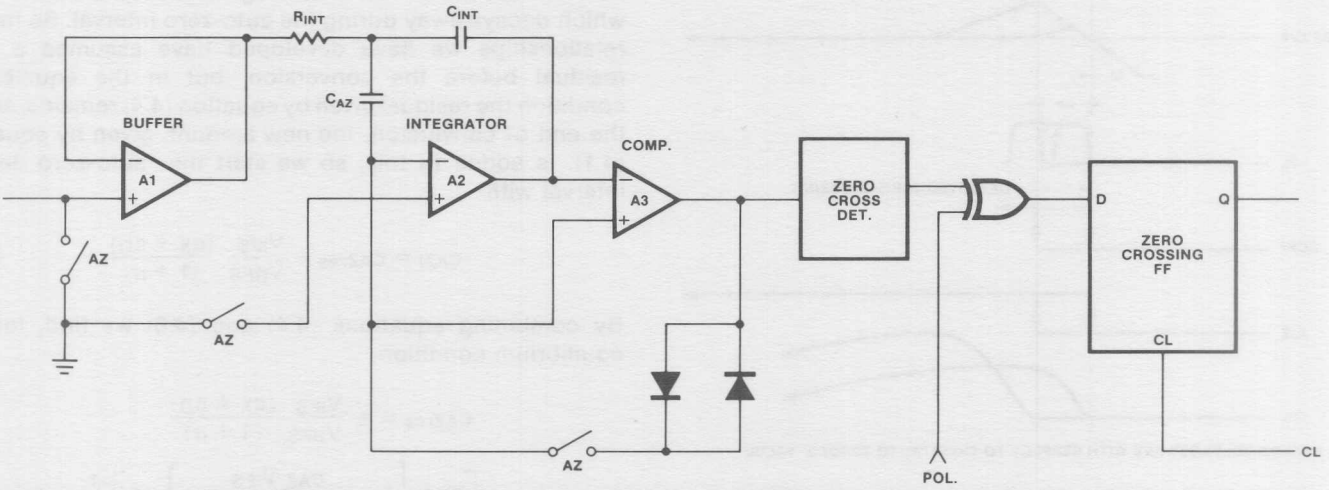

Figure 7. The Analog System (simplified to show only Auto-Zero connections)

This voltage will decay with a time constant controlled by the integrating resistor and the two capacitors, while the auto-zero capacitor is easily kept in step owing to the high comparator gain. Thus, at the end of the auto-zero time, $t_{AZ} = c_{AZ}\, t_{cp}$, the residual will be reduced to:

$$V_{AZres} = V_{AZI} \exp\left(\frac{-(c_{AZ})(t_{cp})}{R_{INT}(C_{INT}+C_{AZ})}\right)$$

$$= V_{Ires}\left(\frac{C_{INT}}{C_{AZ}+C_{INT}}\right)\exp\left(\frac{(-c_{AZ})(t_{cp})}{R_{INT}(C_{INT}+C_{AZ})}\right)$$

For the residual left after a zero-crossing, we may further refine this to:

$$V_{AZres} = V_{IFS}\left(\frac{c_X + c_D}{c_{FS}}\right)\frac{C_{INT}}{(C_{AZ}+C_{INT})} \exp\left(\frac{-c_{AZ}\, t_{cp}}{R_{INT}(C_{INT}+C_{AZ})}\right) \quad \textbf{(4.2)}$$

For the overrange case, we may again assume a large negative c_X value.

Now $R_{INT}\, C_{INT}$ is controlled by the buffer swing, V_{BFS}, the integrator swing, V_{IFS}, and the integration time $t_{INT} = c_{INT}\, t_{cp}$, so that

$$V_{BFS}/R_{INT} \cdot t_{INT} = C_{INT}\, V_{IFS}, \text{ or } R_{INT}\, C_{INT} = c_{INT}\frac{V_{BFS}}{V_{IFS}}\, t_{cp}$$

Also we may write $C_{AZ} = \alpha\, C_{INT}$, for convenience, and will then obtain

$$V_{AZres} = V_{Ires}\left(\frac{1}{1+\alpha}\right)\exp\left(\frac{-c_{AZ}\, V_{IFS}}{c_{INT}\, V_{BFS}\,(1+\alpha)}\right) \quad \textbf{(4.3)}$$

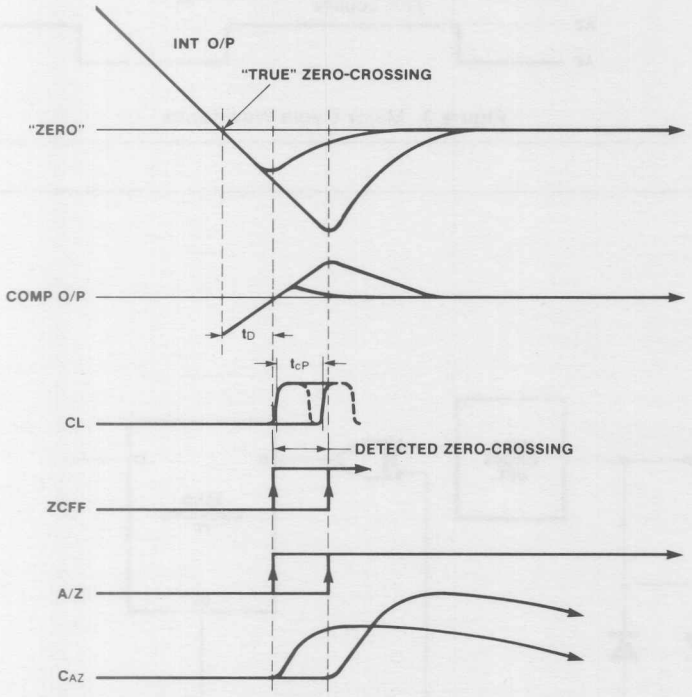

Figure 9. Waveforms at Beginning of Auto-Zero Interval

This residual voltage on the auto-zero capacitor effectively increases the magnitude of the input voltage as seen on the output of the buffer. Thus, converting this voltage to count-equivalents,

$$c_{AZres} = \frac{V_{AZres}}{V_{BFS}} \cdot c_{FS} = \frac{V_{IFS}}{V_{BFS}}\frac{(c_X + c_D)}{(1+\alpha)} \exp\left(-\frac{c_{AZ}}{c_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+\alpha}\right) \quad \textbf{(4.4)}$$

Since this voltage also subtracts from the reference, its effect at the input is magnified in the ratio

$$c_{INres} = c_{AZres}\left(\frac{c_{INT}+c_{DE}}{c_{INT}}\right) \text{ so that}$$

$$c_{INres} = \left(1+\frac{c_{DE}}{c_{INT}}\right)\left(\frac{V_{IFS}}{V_{BFS}}\right)\frac{(c_X+c_D)}{(1+\alpha)} \exp\left(-\frac{c_{AZ}}{c_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+\alpha}\right) \quad \textbf{(4.5)}$$

Note that c_{DE} is equal to the displayed result, except for over-range conditions, when it is equal to c_{FS} and the first bracket becomes 3. Also, $c_{AZ} = c_{INT}$; and this expression, so substituted, determines the overrange residual performance.

For the normal in-range condition, two things should be noted here. First, this residual acts to increase the input voltage magnitude, and secondly, a small increase in input voltage tends to decrease the magnitude of the residual (until the result count changes). These effects lead to "stickyness" in the readings; suppose, in a noise-free system, that the input voltage is at a level where the residual is a minimum; the detected zero-crossing follows the true one as closely as possible. A minute increase in input voltage will cause the zero-crossing to be detected one pulse later, and the residual to jump to its maximum value. The effect of this is a small increase in the apparent input voltage; thus if we now remove the minute increase, the residual voltage effect will maintain the new higher reading; in fact we will have to reduce the input voltage by an amount commensurate with the effective residual voltage to force the reading to drop back to the lower value. In more detail, we should consider the equilibrium conditions on the auto-zero capacitor. Clearly, the voltage added at the end of reference integrate must just balance that which decays away during the auto-zero interval. So far the relationships we have developed have assumed a zero residual before the conversion, but in the equilibrium condition the residual given by equation (4.4) remains, and at the end of conversion, the new amount, given by equation (4.1), is added to this, so we start the "auto-zero decay" interval with

$$c_{AZI} = c_{AZres} + \frac{V_{IFS}}{V_{BFS}}\frac{(c_X+c_D)}{(1+\alpha)} \quad \textbf{(4.6)}$$

By combining equations (4.4) and (4.6) we find, for the equilibrium condition,

$$c_{AZres} = \pm\frac{V_{IFS}}{V_{BFS}}\frac{(c_X+c_D)}{(1+\alpha)} \left[\exp\left\{+\frac{c_{AZ}\, V_{IFS}}{c_{INT}\, V_{BFS}\,(1+\alpha)}\right\} - 1\right]^{-1}$$

Once again, the effect of this at the input is multiplied by the ratio of total input integrate times, so that, under equilibrium conditions,

$$C_{INres} = \pm \frac{V_{IFS}}{V_{BFS}} \left(1 + \frac{C_{DE}}{C_{INT}}\right) \frac{(C_X + C_D)}{(1+\alpha)} \left[\exp\left\{\frac{C_{AZ}\, V_{IFS}}{C_{INT}\, V_{BFS}\,(1+\alpha)}\right\} - 1\right]^{-1} \quad \textbf{(4.7)}$$

Those expert at skipping to the end of the difficult bit will recognize that as the final equation, in terms of complexity. So let us now see what it means. Clearly, the error term is greater, the larger C_{DE}/C_{INT}, and the smaller C_{AZ}/C_{INT}. For the devices considered here (except some applications of the ICL7109) these are both worst case near full scale input, where $C_{DE}/C_{INT} \approx 2$ and $C_{AZ}/C_{INT} \approx 1$.

Substituting these, we find the worst case

$$C_{INres} \simeq \pm \frac{V_{IFS}}{V_{BFS}} (3) \frac{(C_X + C_D)}{(1+\alpha)} \left[\exp\left\{\frac{V_{IFS}}{V_{BFS}\,(1+\alpha)}\right\} - 1\right]^{-1} \quad \textbf{(4.8)}$$

Recall that C_D is fixed; and C_X must be between 0 and 1. The expression is now a function purely of the ratio of integrator and buffer full scale swings, and the ratio of auto-zero and integrator capacitors, α. The effect of the latter ratio is mixed; a larger value reduces the initial error, but increases the time — constant for its decay. The relationship is plotted in Figure 10 and shows the desirability of keeping the integrator swing higher than the buffer swing. Note also that a lower capacitance ratio α always improves the residual. However, both noise and the common-mode effects discussed in Section 3 above require a large auto-zero capacitor, and a compromise must be reached. In general, if the full scale input is small, a large C_{AZ} is needed, but for larger full scale inputs, a smaller value is best. Note also that the comparator delay (C_D in equation (4.8)) is also effectively enhanced. This has the effect of shrinking the zero somewhat more than

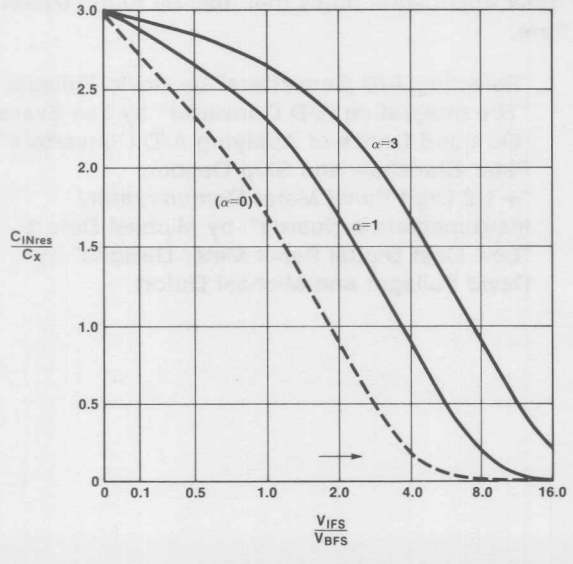

Figure 10. Auto-Zero Loop Residual vs. Integrator/Buffer Swing and Capacitor Ratios (worst case)

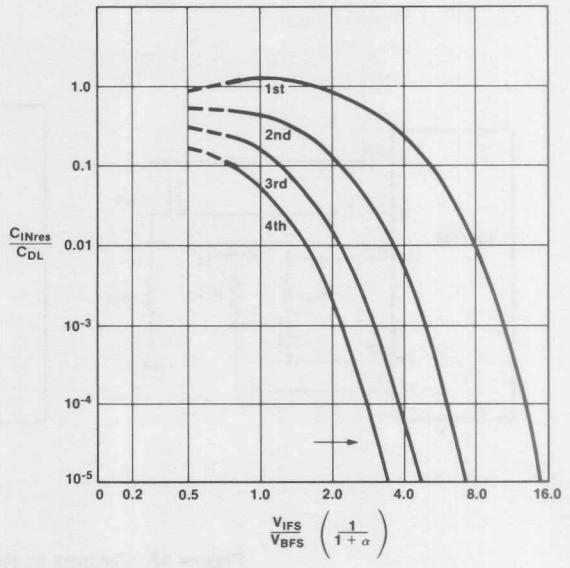

Figure 11. Auto-Zero Loop Residual vs. Integrator/Buffer Swing for Overload and Capacitor Ratio

normally occurs. Since this term changes sign with polarity, the converter will have a tendency to keep the current sign at zero input.

The effects of noise should be mentioned here. The worst case value of residual shown in Figure 10 assumes a very gradual approach to equilibrium, and any noise spike causing the reading to flash to the next value will destroy this carefully established residual value! Thus, for any system with noise of 1/3 count or more, the effect is greatly reduced, and even 1/10 count of noise will restrict the actual hysteresis value found in practice. The detailed analysis of the auto-zero residual problem in the presence of appreciable noise is left as an exercise for the masochist.

For overrange conditions, the controlling equation is (4.5) with the appropriate substitutions for the count ratios. Specifically, putting C_{OR} for the count-equivalent value of the overrange above full scale, and ignoring C_D, we obtain:

$$C_{INres} = 3 \left(\frac{V_{IFS}}{V_{BFS}}\right) \left(\frac{C_{OR}}{1+\alpha}\right) \exp\left[-\frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+\alpha}\right] \quad \textbf{(4.9)}$$

This is plotted in Figure 11, and shows the very strong dependence on the integrator to buffer swing ratio. The direction is the opposite of that for the post-zero-crossing residual, as well as being normally much larger. A positive overrange on one reading will tend to make the next reading(s) too negative, and vice versa. The influence on second and even subsequent readings after an overrange can also be appreciable in some cases. The miss-charge trapped on the auto-zero capacitor during the first conversion after an overrange will still be there at the end. If this conversion is in-range, we may ignore C_X and C_D and just consider the continuation of the exponential decay during the following Auto-Zero phase. Thus, at the beginning of the second conversion, the residual will have been reduced to:

$$C_{AZres\ 2} = C_{AZres} \exp\left[-\frac{C_{AZ}}{C_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+\alpha}\right]$$

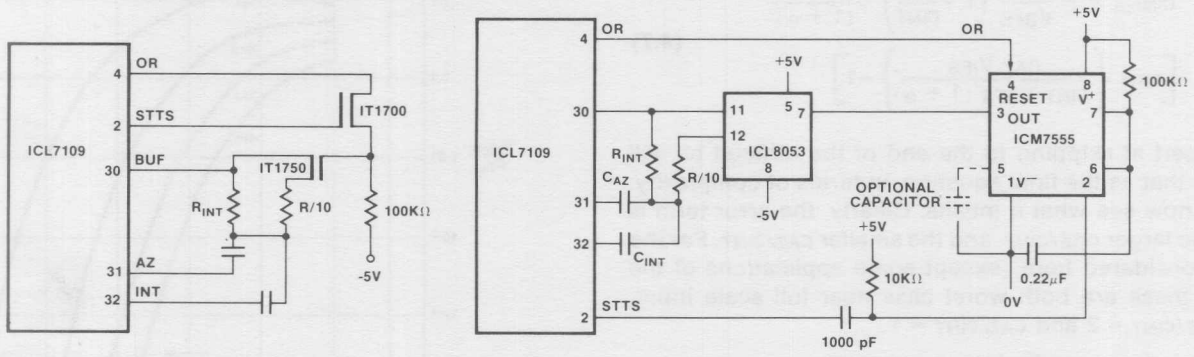

Figure 12. Circuits to Reduce Overrange Residual on ICL7109

where c_{AZres} is given by equation (4.4). This will be similar for subsequent in-range conversions. The effect at the input is again increased by the time ratio of DE-integrate and INTegrate, and so we may write, for the effective error at the input on the nth conversion after the overrange:

$$c_{INres_n} = \left(1 + \frac{C_{DE}}{C_{INT}}\right)\left(\frac{V_{IFS}}{V_{BFS}}\right)\left(\frac{C_{OR}}{1+\alpha}\right)\left[\exp\left(-\frac{C_{AZ}}{C_{INT}} \cdot \frac{V_{IFS}}{V_{BFS}} \cdot \frac{1}{1+\alpha}\right)\right]^n \quad \textbf{(4.10)}$$

This also is plotted in Figure 11, for various values of n against $\frac{V_{IFS}}{V_{BFS}} \frac{1}{1+\alpha}$, for worst case conditions (an overload followed by several full scale conversions).

The residual can be reduced for devices, such as the ICL7109, which provide indications of overrange conversions and auto-zero phase (OR and STATUS in the ICL7109) by reducing the integrator time constant during all or part of the Auto-Zero phase after an overrange conversion. This can be done by shorting out all or part of the integrating resistor R_{INT} by a suitable analog switch. A circuit to do this is shown in Figure 12 for the ICL7109. Care should be taken to ensure that the switch does not cause errors due to charge injection into the capacitors when going OFF. Alternatively the clock can be slowed down or stopped, or Run/$\overline{\text{Hold}}$ used to extend the Auto-Zero phase under the same conditions. These techniques are much harder to apply to devices such as the ICL7106/7 which do not provide the necessary signals. Generally, however, these devices are not used in multiplexing applications.

SUMMARY

This note has described the most common behavior patterns that cause concern and/or confusion among users of the ICL7106/7 and similar products, and their origins. Hopefully, it will help alleviate or eliminate any consequent applications problems with this family of devices. Naturally, some parts will not show all of the effects; for instance, the ICL7116/7 and ICL7135 cannot suffer from large common-mode voltages between reference and COMMON, because no such voltage can be applied, and the ICL7135 has a modified auto-zero sequence that alters the residual effects of Section 4.

Some other application notes that may be found useful are listed here:

A016	"Selecting A/D Converters" by David Fullagar
A017	"The Integrating A/D Converter" by Lee Evans
A018	"Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
A019	"4-1/2 Digit Panel Meter Demonstrator/ Instrumentation Boards", by Michael Dufort
A023	"Low Cost Digital Panel Meter Designs" by David Fullagar and Michael Dufort

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